

CLAIMS

1        1. A buffer circuit comprising:  
2        a driver device;  
3        an input device to receive a first set of signals and to  
4        produce a second set of signals, said driver device to receive  
5        said second set of signals and to output a third set of  
6        signals based on said second set of signals input to said  
7        driver device; and

8        a comparing device to receive said third set of signals  
9        from said driver device and to produce a fourth set of signals  
10       based on said third set of signals, said comparing device to  
11       compare said fourth set of signals with said first set of  
12       signals.

1       2. The buffer circuit of claim 1, wherein said input  
2       device comprises a plurality of first multiplexor devices to  
3       receive said first set of signals and at least a plurality of  
4       latch devices to receive outputs from said plurality of first  
5       multiplexor devices.

1       3. The buffer circuit of claim 2, wherein said input  
2       device further comprises a second multiplexor device to couple  
3       to an output of each of said plurality of latch devices, and a  
4       latch device to couple to an output of said second multiplexor  
5       device and to an input of said driver device.

1           4. The buffer circuit of claim 3, wherein said plurality  
2 of latch devices operate based on a first clock signal, and  
3 said latch device operates based on a second clock signal,  
4 said second clock signal being faster than said first clock  
5 signal.

1           5. The buffer circuit of claim 1, wherein said comparing  
2 device comprises a first plurality of logic circuits and a  
3 plurality of latch devices, said plurality of latch circuits  
4 to output said fourth set of signals to inputs of said first  
5 plurality of logic circuits, said first plurality of logic  
6 circuits to further receive said first set of signals as  
7 inputs and to perform a comparison based on said received  
8 first set of signals and said fourth set of signals.

1           6. The buffer circuit of claim 5, wherein said plurality  
2 of latch devices comprises a plurality of flip-flop circuits.

1           7. The buffer circuit of claim 5, wherein said first  
2 plurality of logic circuits comprise a plurality of XOR logic  
3 circuits.

1           8. The buffer circuit of claim 5, further comprising a  
2 second plurality of logic circuits, each to receive an output  
3 from each one of said first plurality of logic circuits.

1           9. The buffer circuit of claim 8, wherein a first one of  
2 said second plurality of logic circuits comprises an AND logic  
3 circuit and a second one of said second plurality of logic  
4 circuits comprises an OR logic circuit.

1           10. The buffer circuit of claim 9, wherein an output of  
2 said AND logic circuit represents an ALL FAIL condition and an  
3 output of said OR logic circuit represents an AT LEAST ONE  
4 FAIL condition.

1           11. The buffer circuit of claim 1, wherein said buffer  
2 circuit is provided on a chip.

1           12. An apparatus for testing a driver device, said  
2 apparatus comprising:

3           an input device to receive a first set of signals and to  
4 provide a second set of signals to said driver device; and

5           a comparing device to receive a third set of signals  
6 output from said driver device and to produce a fourth set of  
7 signals, said comparing device to further receive said first  
8 set of signals from said input device and to compare said  
9 first set of signals with said fourth set of signals.

1           13. The apparatus of claim 12, wherein said input device  
2 comprises a plurality of first multiplexor devices to receive  
3 said first set of signals and at least a plurality of latch

4 devices to receive outputs from said plurality of first  
5 multiplexor devices.

1 14. The apparatus of claim 13, wherein said input device  
2 further comprises a second multiplexor device to couple to an  
3 output of each of said plurality of latch devices, and a latch  
4 device to couple to an output of said second multiplexor  
5 device and to an input of said driver device.

1 15. The apparatus of claim 14, wherein said plurality of  
2 latch devices operate based on a first clock signal, and said  
3 latch device operates based on a second clock signal, said  
4 second clock signal being faster than said first clock signal.

1 16. The apparatus of claim 12, wherein said comparing  
2 device comprises a first plurality of logic circuits and a  
3 plurality of latch devices, said plurality of latch circuits  
4 to output said fourth set of signals to inputs of said first  
5 plurality of logic circuits, said first plurality of logic  
6 circuits to further receive said first set of signals as  
7 inputs and to perform a comparison based on said received  
8 first set of signals and said fourth set of signals.

1 17. The apparatus of claim 16, wherein said plurality of  
2 latch devices comprises a plurality of flip-flop circuits.

1 18. The apparatus of claim 16, wherein said first  
2 plurality of logic circuits comprise a plurality of XOR logic  
3 circuits.

1 19. The apparatus of claim 16, further comprising a  
2 second plurality of logic circuits, each to receive an output  
3 from each one of said first plurality of logic circuits.

1 20. The apparatus of claim 16, wherein a first one of  
2 said second plurality of logic circuits comprises an AND logic  
3 circuit and a second one of said second plurality of logic  
4 circuits comprises an OR logic circuit.

1 21. The apparatus of claim 20, wherein an output of said  
2 AND logic circuit represents an ALL FAIL condition and an  
3 output of said OR logic circuit represents an AT LEAST ONE  
4 FAIL condition.

1 22. The apparatus of claim 21, further comprising a  
2 device to determine a difference in time between the AT LEAST  
3 ONE FAIL CONDITION and the ALL FAIL CONDITION, said device to  
4 compare said determined difference with a predetermined  
5 difference to determine if said driver device is defective.

1 23. The apparatus of claim 12, wherein each of said  
2 fourth set of signals is delayed based on strobe signals.

1           24. The apparatus of claim 12, wherein said apparatus is  
2 provided on a chip with said driver device.

1           25. A method of testing a driver device, said method  
2 comprising:  
3           receiving a first set of signals at a first component;  
4           transmitting a second set of signals from said first  
5 component to said driver device, said second set of signals  
6 being based on said first set of signals;  
7           receiving a third set of signals from said driver device;  
8           providing a fourth set of signals and said first set of  
9 signals to a second component, said fourth set of signals  
10 being based on said third set of signals; and  
11           comparing said fourth set of signal with said first set  
12 of signals at said second component.

1           26. The method of claim 25, further comprising delaying  
2 each one of said third plurality of signals so as to provide  
3 signals corresponding to said fourth set of signals.

1           27. The method of claim 25, wherein said first component,  
2 said second component and said driver device are all provided  
3 on a chip.

1           28. The method of claim 25, further comprising outputting  
2 a first signal when one of said fourth set of signals does not  
3 match a corresponding one of said first set of signals.

1           29. The method of claim 28, further comprising outputting  
2   a second signal when all of said fourth set of signals do not  
3   match corresponding ones of said second set of signals.

1           30. The method of claim 29, further comprising comparing  
2   a time difference between said first signal and said second  
3   signal with a predetermined time difference so as to determine  
4   if said driver device is defective.